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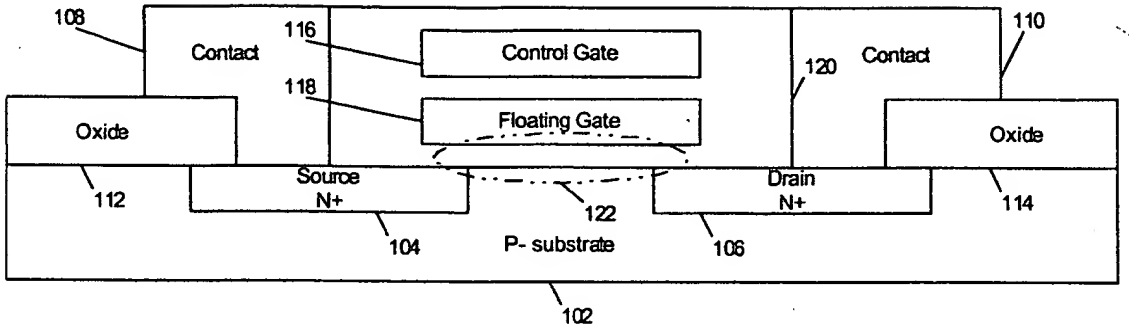

Figure 1A
(Prior Art)

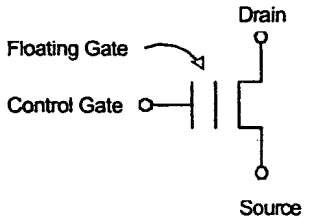

Figure 1B
(Prior Art)

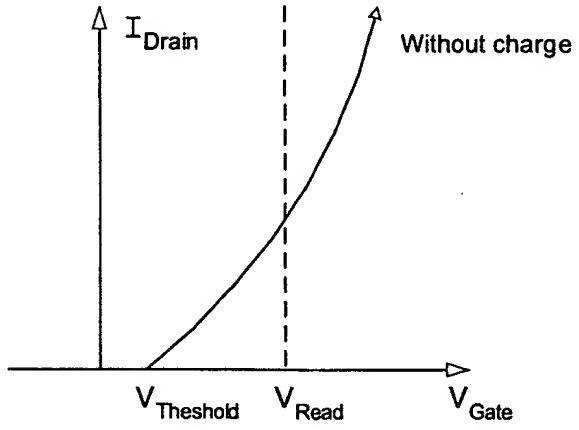

Figure 1C
(Prior Art)

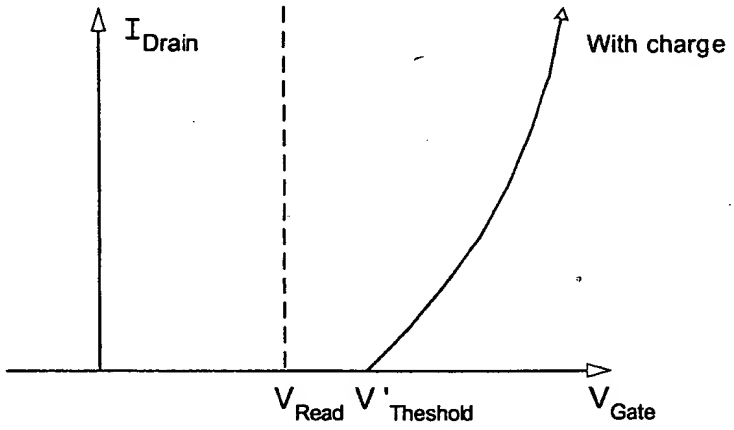

Figure 1D
(Prior Art)

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Calculation of nv memory cell retention characteristics

	m0, kg	kb, J/K	h, J-s	hb, J-s
q, C	9.1095E-031	1.38062E-023	6.62617E-034	1.054588E-034
1.6022E-019				

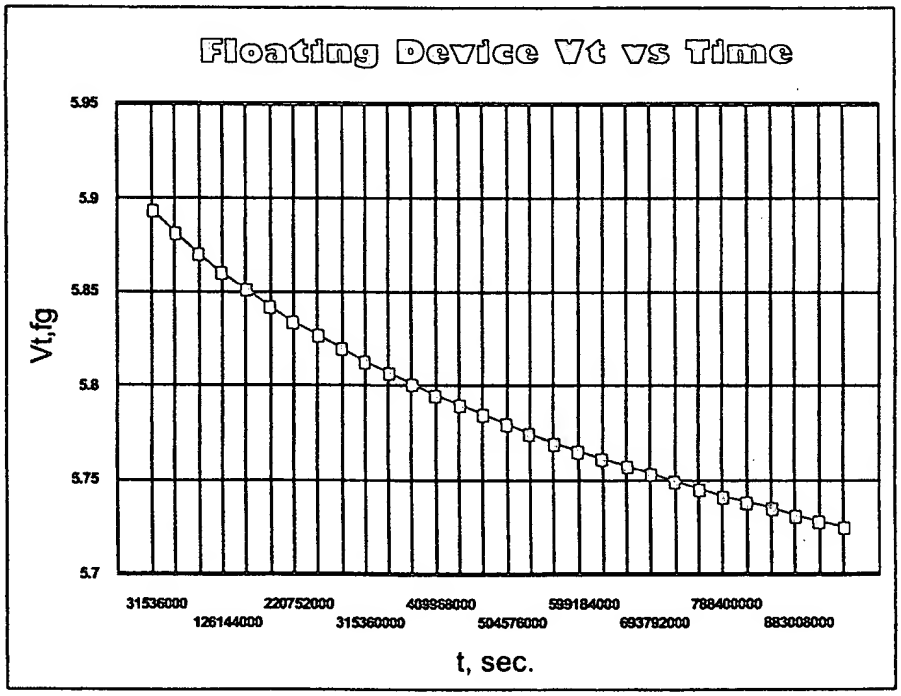
eV (barrier)	ε1	mr, effective mass ratio	T, K degree
2.9	3.9	0.5	300

C	b
1.0630E-006	2.3854E+008

Seconds	Time Period
31536000	1 year
94608000	3 years
1.89E+008	6 years
2.84E+017	9 years
3.78E+008	12 years
4.73E+008	15 years
9.08E+009	18 years
6.62E+008	21 years
7.57E+008	24 years
8.51E+008	27 years
9.46E+008	30 years

Lfg um	0.6000	Channel length of floating gate device
Wfg um	1000.0000	Channel width of floating gate device.
Hfg um	0.0900	Thickness of floating gate polysilicon conductor
Wrx um	0.5000	Width of floating gate overlapping shallow trench isolation
Ttunox A	80	Tunnel oxide thickness
Tono A	190	Thickness of Oxide-Nitride-Oxide dielectric between floating gate and control gate for capacitive coupling
Tswox A	300	Thickness of sidewall oxide between floating gate and control gate for sidewall coupling
Xfd um	0.0500	Length of floating gate overlapping drain region of the floating gate MOSFET
Xfs um	0.3500	Length of floating gate overlapping source region of the floating gate MOSFET
Ainj um2	0.0438	Area of the electron tunneling region between the floating gate and the source for resetting the floating gate charge
Cfc fF	1089.5358	Capacitance between the floating gate and the control gate
Cfsx fF	0.4313	Capacitance between the floating gate and the silicon substrate
Cfd fF	0.1078	Capacitance between the floating gate and the drain
Cfs fF	0.7547	Capacitance between the floating gate and the source
Cfg fF	1090.8295	Total floating gate capacitance
Cr,wl	0.9988	Control gate to floating gate coupling ratio
Cr,src	0.0007	Source junction to floating gate coupling ratio
Vt,fg V	0.90	Threshold voltage of floating gate MOSFET
Verase	0.00	Erase voltage applied to the source(not used here, set to zero)
Vfg,ini	-5.00	Initial floating chaged voltage
Va	0.00	Actual erase volatge (equal to applied + charge stored on the floating)
S	3.76E+016	Derived parameter in the floating gate "erase" equation
X	1.27E+011	Derived parameter in the floating gate "erase" equation

t, sec.	Vt,fg
0.00001	5.907
31536000	5.894
63072000	5.882
94608000	5.871
1.26E+008	5.861
1.58E+008	5.852
1.89E+008	5.843
2.21E+008	5.835
2.52E+008	5.827
2.84E+008	5.820
3.15E+008	5.814
3.47E+008	5.807
3.78E+008	5.801
4.1E+008	5.795
4.42E+008	5.790
4.73E+008	5.785
5.05E+008	5.780
5.36E+008	5.775
5.68E+008	5.770
5.99E+008	5.766
6.31E+008	5.762
6.62E+008	5.757
6.94E+008	5.753
7.25E+008	5.750
7.57E+008	5.746
7.88E+008	5.742
8.2E+008	5.739
8.51E+008	5.735
8.83E+008	5.732
9.15E+008	5.729
9.46E+008	5.726



Figures 1E-1F
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Calculation of nv memory cell retention characteristics

qe, C	m0, kg	kb, J/K	h, J-s	hb, J-s
1.6022E-019	9.1095E-031	1.38062E-023	6.62617E-034	**********

ϕb, eV (barrier)	εl	mr, effective mass ratio	T, K degree
2.9	3.9	0.5	300

C	b
1.0630E-006	2.3854E+008

Seconds	Time Period
60	1 minute
3600	1 hour
86400	1 day
604800	1 week
2592000	1 month
**********	1 year
**********	4 years
**********	16 years
**********	32 years

Lfg um	0.6000	Channel length of floating gate device
Wfg um	1000.0000	Channel width of floating gate device.
Hfg um	0.0900	Thickness of floating gate polysilicon conductor
Wrx um	0.5000	Width of floating gate overlapping shallow trench isolation
Ttunox A	80	Tunnel oxide thickness
Tono A	190	Thickness of Oxide-Nitride-Oxide dielectric between floating gate and control gate for capacitive coupling
Tswox A	300	Thickness of sidewall oxide between floating gate and control gate for sidewall coupling
Xfd um	0.0500	Length of floating gate overlapping drain region of the floating gate MOSFET
Xfs um	0.3500	Length of floating gate overlapping source region of the floating gate MOSFET
Ainj um2	0.0438	Area of the electron tunneling region between the floating gate and the source for resetting the floating gate charge
Cfc fF	1089.5358	Capacitance between the floating gate and the control gate
Cfsx fF	0.4313	Capacitance between the floating gate and the silicon substrate
Cfd fF	0.1078	Capacitance between the floating gate and the drain
Cfs fF	0.7547	Capacitance between the floating gate and the source
Cfg fF	1090.8295	Total floating gate capacitance
Cr,wl	0.9988	Control gate to floating gate coupling ratio
Cr,src	0.0007	Source junction to floating gate coupling ratio
Vt,fg V	0.90	Threshold voltage of floating gate MOSFET
Verase	0.00	Erase voltage applied to the source(not used here, set to zero)
Vfg,ini	-5.00	Initial floating chaged voltage
Va	0.00	Actual erase volatge (equal to applied + charge stored on the floating)
S	3.76E+016	Derived parameter in the floating gate "erase" equation
X	1.27E+011	Derived parameter in the floating gate "erase" equation

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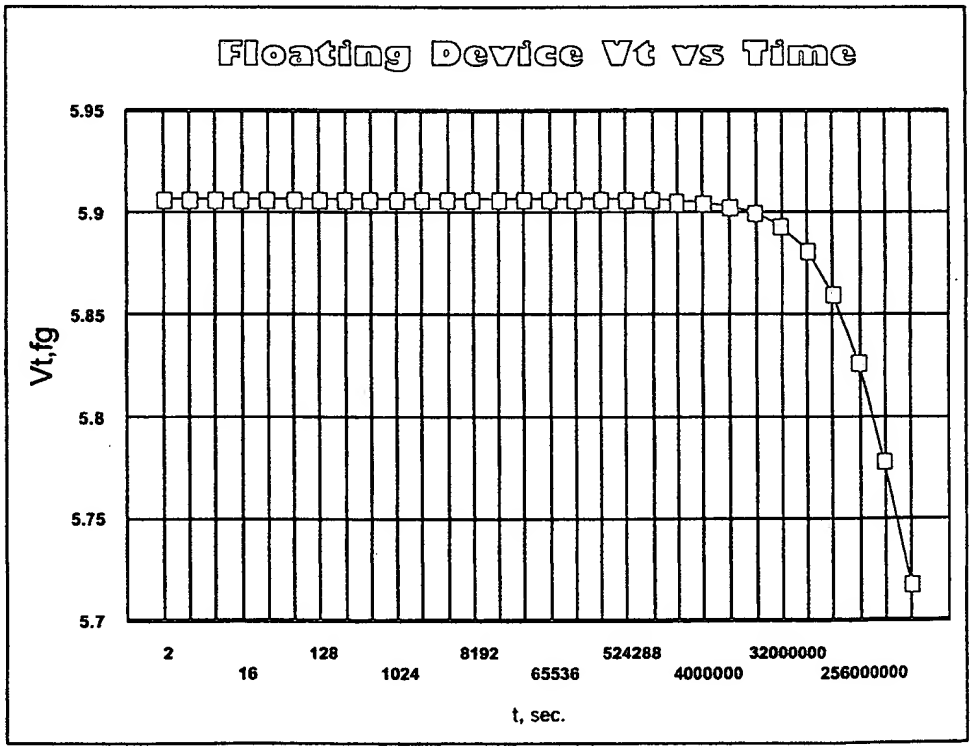
t, sec.	Vt,fg
0.00001	5.907
2	5.907
4	5.907
8	5.907
16	5.907
32	5.907
64	5.907
128	5.907
256	5.907
512	5.907
1024	5.907
2048	5.907
4096	5.907
8192	5.907
16384	5.907
32768	5.907
65536	5.907
131072	5.907
262144	5.907
524288	5.907
1000000	5.907
2000000	5.906
4000000	5.905
8000000	5.904
16000000	5.900
32000000	5.894
64000000	5.881
**********	5.860
**********	5.827
**********	5.779
**********	5.718



Figures 1G-1H
(Prior Art)

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Calculation of nv memory cell retention characteristics

q, C	m0, kg	kb, J/K	h, J-s	hb, J-s
1.6022E-019	9.1095E-031	1.38062E-023	6.62617E-034	**********

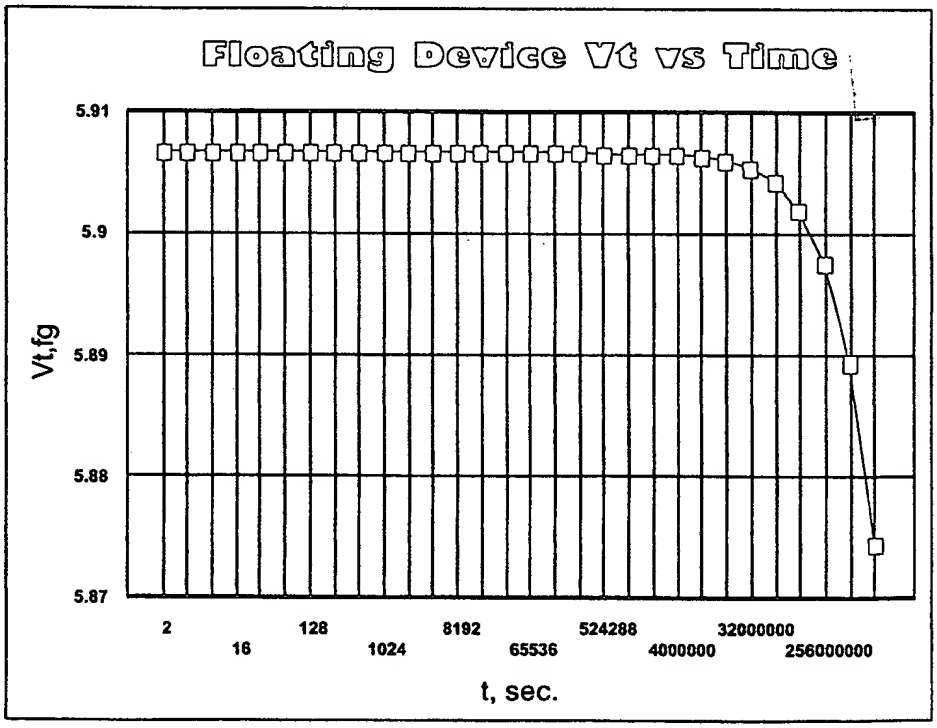
b0, eV (barrier)	ε1	mr, effective mass ratio	T, K degree
2.9	3.9	0.5	300

C	b
1.0630E-006	2.3854E+008

Seconds	Time Period
60	1 minute
3600	1 hour
86400	1 day
604800	1 week
2592000	1 month
**********	1 year
**********	4 years
**********	16 years
**********	32 years

Lfg um	0.6000	Channel length of floating gate device
Wfg um	1000.0000	Channel width of floating gate device.
Hfg um	0.0900	Thickness of floating gate polysilicon conductor
Wrx um	0.5000	Width of floating gate overlapping shallow trench isolation
Ttunox A	85	Tunnel oxide thickness
Tono A	190	Thickness of Oxide-Nitride-Oxide dielectric between floating gate and control gate for capacitive coupling
Tswox A	300	Thickness of sidewall oxide between floating gate and control gate for sidewall coupling
Xfd um	0.0500	Length of floating gate overlapping drain region of the floating gate MOSFET
Xfs um	0.3500	Length of floating gate overlapping source region of the floating gate MOSFET
Ainj um2	0.0438	Area of the electron tunneling region between the floating gate and the source for resetting the floating gate c
Cfc fF	1089.5358	Capacitance between the floating gate and the control gate
Cfsx fF	0.4059	Capacitance between the floating gate and the silicon substrate
Cfd fF	0.1015	Capacitance between the floating gate and the drain
Cfs fF	0.7103	Capacitance between the floating gate and the source
Cfg fF	1090.7534	Total floating gate capacitance
Cr,wl	0.9989	Control gate to floating gate coupling ratio
Cr,src	0.0007	Source junction to floating gate coupling ratio
Vt,fg V	0.90	Threshold voltage of floating gate MOSFET
Verase	0.00	Erase voltage applied to the source(not used here, set to zero)
Vfg,ini	-5.00	Initial floating chaged voltage
Va	0.00	Actual erase volatge (equal to applied + charge stored on the floating)
S	4.09E+017	Derived parameter in the floating gate "erase" equation
X	1.20E+011	Derived parameter in the floating gate "erase" equation

t, sec.	Vt,fg
0.00001	5.907
2	5.907
4	5.907
8	5.907
16	5.907
32	5.907
64	5.907
128	5.907
256	5.907
512	5.907
1024	5.907
2048	5.907
4096	5.907
8192	5.907
16384	5.907
32768	5.907
65536	5.907
131072	5.907
262144	5.907
524288	5.907
1000000	5.907
2000000	5.907
4000000	5.906
8000000	5.906
1.6E+007	5.906
3.2E+007	5.905
6.4E+007	5.904
**********	5.902
**********	5.898
**********	5.889
**********	5.874



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Figures 1I-1J (Prior Art)